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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	09/841,974
Filing Date	4/24/01
First Named Inventor	Terry Lee Goode
Art Unit	2128
Examiner Name	Fred O. Ferris III
Attorney Docket Number	003921.00011

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
FOF		US- 5,649,176	07-15-1997	Selvidge, et al.	
FOF		US- 5,659,716	08-19-1997	Selvidge, et al.	
		US- 5,841,967	11-24-1998	Sample, et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
FOF		JP 1-154251	06-1989			No
FOF		GB 1,444,084	07-28-1976	Cheesman		
FOF		GB 2,182,220	05-07-1987	Austin		

Examiner Signature		Date Considered	8/7/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 2 of 2

Complete If Known	
Application Number	09/841,974
Filing Date	4/24/01
First Named Inventor	Terry Lee Goode
Art Unit	2128
Examiner Name	Fred O. Ferris III
Attorney Docket Number	003921.00011

NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
FF		Kronstadt, et al., "Software Support for the Yorktown Simulation Engine," 19th Design Automation Conference, Paper 7.3, 1982, pp. 60-64	
FF		Koike, et al., "HAL: A High-Speed Logic Simulation Machine," IEEE Design & Test, Oct. 1985, pp. 61-73	
FF		Shear, "Tools Help you Retain the Advantages of Using Breadboards in Gate-Array Design," EDN, Mar. 18, 1987, pp. 81-88	
FF		J.W. Babb, "Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulation," Masters Thesis, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science, Nov. 1993; Also available as MIT/LCS Technical Report TR-686	
FF		M. Dahl, J. Babb, R. Tessier, S. Hanono, D. Hoki, and A. Agarwal, "Emulation of the Sparcle Microprocessor with the MIT Virtual Wires Emulation System, " IEEE Workshop on FPGAs for Custom Computing Machines '94 (FCCM '94), Apr. 1994	
FF		R. Tessier, J. Babb, M. Dahl, D. Hanono and A. Agarwal, "The Virtual Wires Emulation System: A Gate-Efficient ASIC Prototyping Environment," ACM Workshop on FPGA's (FPGA '94), Feb. 1994	
FF		J. Babb, R. Tessier, and A. Agarwal, "Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulators," IEEE Workshop on FPGAs for Custom Computing Machines '93 (FCCM '93), Apr. 1993	
FF		IKOS Systems to Acquire Virtual Machine Works; IKOS Systems Mar. 11, 1996	
FF		R. Goering, "Emulation for the Masses," Electronic Engineering Times, Jan. 1996	
FF		J. Babb, R. Tessier, and A. Agarwal, "Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulators," Massachusetts Institute of Technology, Student Workshop on Scalable Computing, August 4, 1993	
FF		R. Tessier, J. Babb, M. Dahl, D. Hanono, and D. Hoki, "The Virtual Wires Emulation System; A Gate-Efficient ASIC Prototyping Environment," MIT Student Workshop on Scalable Computing; July 21-22, 1994	
FF		Feng, "A Survey of Interconnection Networks," Computer, Dec. 1981, pp. 12-27	
FF		Chapter 36, "Switching Networks and Traffic Concepts," Reference Data for Radio Engineers, Howard W. Sams & Co., 1981, pp. 36-1 to 36-16	
FF		S. Hanono, "Inner View Hardware Debugger: A Logic Analysis Tool for the Virtual Wires Emulation System," Masters Thesis, MIT Department of Electrical Engineering and Computer Science, Jan. 1995; Also available as MIT/LCS Technical Report.	

Examiner Signature		Date Considered	8/7/05

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